

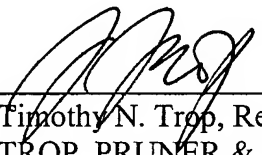
## REMARKS

Claim 1 has been amended to include the subject matter of former dependent claim 3. That claim was rejected under Section 102 or Section 103 over a single reference to Giovannetti. However, Giovannetti does not teach a two-stage response to temperature. In the two-stage response set forth in the claims, at a first temperature, lower than a second temperature, the operation of the device is adjusted and then at the second higher temperature, the cache is changed from write-back to write-through. None of the material cited supports this two-stage operation. All that Giovannetti talks about is transitioning from write-back to delayed write.

Therefore, reconsideration is respectfully requested.

Respectfully submitted,

Date: November 17, 2006



---

Timothy N. Trop, Reg. No. 28,994  
TROP, PRUNER & HU, P.C.  
1616 South Voss Road, Suite 750  
Houston, TX 77057-2631  
713/468-8880 [Phone]  
713/468-8883 [Fax]

Attorneys for Intel Corporation